UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/023,165	12/18/2001	Franciscus Petrus Widdershoven	NL000722	5094

65913 7590 07/19/2007

NXP, B.V.
NXP INTELLECTUAL PROPERTY DEPARTMENT
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
CHERY, MARDOCHEE	

ART UNIT	PAPER NUMBER
2188	

NOTIFICATION DATE	DELIVERY MODE
07/19/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/023,165
Filing Date: December 18, 2001
Appellant(s): WIDDERSHOVEN, FRANCISCUS PETRUS

Michael Ure
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed May 21, 2007 appealing from the Office action mailed May 9, 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

4691299	Rivest	1987
6,069,827	Sinclair	2000
6,772,274	Estakhri	2004

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rivest (US 4,691,299), Sinclair (US 6,069,827), and Estakhri (US 6,772,274).

As in claim 1, Rivest teaches a system comprising:

a memory having locations, each capable of storing a WOM codeword from a WOM code (Fig. 3, element 28; column 3, lines 31-68; column 5, lines 25-28);

a memory selector for selecting a currently selected location of the locations (Fig. 3, elements 22 and 26., column 3, lines 51-58; column 5, lines 23-35); and

a data encoder that encodes a received data value in a new codeword from the WOM code, as a function of the received data value and a previous codeword stored in the currently selected location, the data encoder causing the currently selected location to be changed to a next one in the logical series when the WOM code is exhausted, the data encoder storing the new codeword in the currently selected location (Fig. 3, element 16; column 3, lines 51-58; column 5, lines 7-35).

Rivest does not explicitly teach a logical series of the locations as recited in claim 1.

Estakhri teaches a flash memory system wherein memory location stores the designation identifying the Current sector associated with the predetermined range of logical block addresses corresponding with the memory location (column 18, lines 5-30).

Regarding claim 1, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use a logical series of the locations as taught by Estakhri in the system of Rivest because it was well known to reduce inefficiencies associated with keeping track of logical block address to physical block address correlation (column 8, lines 57-60).

Rivest further does not explicitly teach a reset circuit that resets the contents of the logical series when the WOM code is exhausted for all locations in the series as recited by claim 1.

Sinclair teaches an erasable write-once type memory where the storage locations are arranged as blocks (i.e. logical series of memory locations), and a storage location once written may not be written again before it is erased (i.e. it is exhausted) (Fig. 2; column 5, lines 8-17).

Sinclair further teaches a wear-leveling technique in which a previously exhausted storage location is not reused until all other storage locations are subsequently used, whereupon when all locations in a block are exhausted, the block is erased (Fig. 3; column 6, lines 7-61).

Regarding claim 1, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to reset the contents of a logical series of locations when writing to the locations is exhausted as taught by Sinclair, in the system of Rivest, in accordance with providing wear-leveling as taught by Sinclair, where utilizing an erasable write-once type memory as taught by Sinclair in the system of Rivest would have been obvious due to the similar nature of the problems to be solved, namely to provide write-once non-volatile storage, and also in view of the advantages provided by reusability.

Claim 2 is rejected using the same rationale as for the rejection of claim 1, where it is readily apparent in Rivest that a memory location is exhausted when it contains a second-generation code (Figs. 1 and 2., column 4, lines 16-32), and that unused locations contain an initial codeword (Rivest, column 3, lines 47-51), where it is further apparent that the erasing operation of Sinclair would produce the same initial codeword as in Rivest.

As to claim 3, it is noted that except for the addition of error correction coding (ECC) of the input data word, claim 3 is equivalent to claim 1 for the trivial case of N=I. Furthermore, although the combination of Rivest and Sinclair does not explicitly teach applying ECC to the input data words, Examiner takes Official Notice that utilizing ECC in non-volatile storage devices is well known in the art as a means to detect and/or correct errors caused by bit failures. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to encode the data word of Rivest and Sinclair using ECC.

Claim 4 is rejected using the same rationale as for the rejection of claim 1, further noting that Sinclair teaches a plurality of blocks (i.e. a series of logical series) (Fig. 3), both Rivest and Sinclair teach addressable memories (Rivest, column 1, lines 15-32; Sinclair, column 4, lines 45-61), where it is apparent that the series selected for an operation is determined under control of the address.

(10) Response to Argument

Appellant's arguments on page 6 and page 7, paragraph 1, that "in Rivest, there is no identification of a logical series of multiple memory locations" and that "Sinclair also fails to teach or suggest the logical series of multiple memory locations" are clearly erroneous.

First of all, the combination of Rivest, Sinclair, and Estakhri is relied upon for the teaching of the claims and Estakhri clearly discloses "selecting a location of a logical series of locations", by disclosing identifying a current sector of a plurality of sectors and each sector is associated with a range of logical block addresses (see column 18, lines 5-30). Thus, it can be clearly seen that the combination of Rivest, Sinclair, and Estakhri discloses the limitation as claimed by applicant.

Appellant's argument on page 7, paragraphs 2-4, that "Estakhri does not contain any relevant teaching about the manner in which data itself is stored and does not identify in advance a series of locations for use in storing successive versions of a piece of data in the manner recited in claim 1" is respectfully traversed.

While the combination of Rivest, Sinclair, and Estakhri is relied upon in the rejection of the claims, Rivest clearly teaches a mapping method for serial or parallel transfer that determines whether a current location can be overwritten or rewritten (see

column 5, lines 7-35). By constantly keeping a mapping of locations that can be rewritten or overwritten, Rivest clearly discloses identifying the locations for writing in advance.

Furthermore, In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., identify in advance a series of locations for use in storing successive versions of a piece of data) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Additionally, in response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Mardochee Chery
Examiner

Conferees:

Hyung Sough
Supervisory Patent Examiner
7/09/07

Lynne H. Browne
Appeal Practice Specialist, TQAS